



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/917,573	07/27/2001	Thomas Marra	262/090	1029

7590

07/30/2003

DAVID E. BENNETT
COATS & BENNETT P.L.L.C.
1400 CRESCENT GREEN
SUITE 300
CARY, NC 27511

EXAMINER

SHINGLETON, MICHAEL B

ART UNIT

PAPER NUMBER

2817

DATE MAILED: 07/30/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/917,523

Applicant(s)

Marra et al.

Examiner

SHINGLETON

Group Art Unit

2817

— The MAILING DATE of this communication appears on the cover sheet beneath the correspondence address —

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE Three MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- ☒ Responsive to communication(s) filed on 7-1-2003
- ☐ This action is **FINAL**.
- ☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

- ☒ Claim(s) 1-35 is/are pending in the application.
- Of the above claim(s) _____ is/are withdrawn from consideration.
- ☐ Claim(s) _____ is/are allowed.
- ☒ Claim(s) 1-24, 26-35 are rejected.
- ☒ Claim(s) 25 is/are objected to.
- ☐ Claim(s) _____ are subject to restriction or election requirement

Application Papers

- ☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.
- ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.
- ☐ The specification is objected to by the Examiner.
- ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119 (a)-(d)

- ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119 (a)-(d).
- ☐ All ☐ Some* ☐ None of the:
- ☐ Certified copies of the priority documents have been received.
- ☐ Certified copies of the priority documents have been received in Application No. _____.
- ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a))

*Certified copies not received: _____

Attachment(s)

- ☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____ ☐ Interview Summary, PTO-413
- ☐ Notice of Reference(s) Cited, PTO-892 ☐ Notice of Informal Patent Application, PTO-152
- ☐ Notice of Draftsperson's Patent Drawing Review, PTO-948 ☐ Other _____

Office Action Summary

DETAILED ACTION

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the non-inverting amplifier used for the bias circuit must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-4 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Mattila et al. 5,432,473 (Mattila) of record.

Figure 2 of Mattila discloses a biasing circuit for biasing a device used for amplifying a radio frequency (RF) signal (See abstract and column 3), the RF signal comprising an amplitude modulated carrier having an amplitude modulation bandwidth, the biasing circuit having an active element operational amplifier configured as a inverting amplifier N21 having an input and an output, wherein during its operation, i.e. during low and large signal inputs, due to the driver circuits like Q30 the active

Art Unit: 2817

element inherently maintains a relatively low output impedance over a bandwidth comparable to the amplitude modulation bandwidth and a resistor R31 having an input connected to the active element output, wherein a fixed direct current (DC) bias voltage applied at the active element input produces a fixed DC voltage at the resistor input and during the operation of the active element a fixed DC voltage is maintained at the resistor input (See column 4, lines 41-48). Alternatively, the selection of the bandwidth and the resistance value of the driver like Q30 so as to keep the operational amplifier N21 from saturating and thus keeping the output impedance thereof low is merely the selection of the optimum or workable range and as this involves routine skill in the art the selection of the bandwidth and resistance of the driver would have been obvious to one of ordinary skill in the art at the time the invention was made.

Claims 5-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mattila et al. in view of Rubin et al. 4,320,352 (Rubin).

The reasoning as applied to claims 1-4 and the following: Figures 1 and 2 of Mattila disclose an amplifier circuit for amplifying a radio frequency (RF) signal (See abstract and column 3), the RF signal comprising an amplitude modulated carrier having an amplitude modulation bandwidth, having a direct current (DC) bias voltage source (V_{ref} and V_{pwr}), a biasing circuit (Figure 2), the biasing circuit having an active element operational amplifier configured as an inverting amplifier N21 having an input connected to the DC bias voltage source and an output, wherein during its operation, i.e. during low and large signal inputs, due to the driver circuits like Q30 the active element inherently maintains a relatively low output impedance over a bandwidth comparable to the amplitude modulation bandwidth of the RF signal and a resistor R31 having an input connected to the active element output and an output connected to the power amplifier, such that the DC bias voltage source provides a fixed DC voltage at the resistor input, regardless of voltage fluctuations of the RF signal received at the power amplifier. Alternatively, the selection of the bandwidth and the resistance value of the driver like Q30 so as to keep the operational amplifier N21 from saturating and thus keeping the output impedance thereof low is merely the selection of the optimum or workable range and as this involves routine skill in the art the selection of the bandwidth and resistance of the driver would have been obvious to one of ordinary skill in the art at the time the invention was made. Mattila is silent on the power amplifiers 3 having a transistor with an input for receiving the RF signal. Mattila does show generic conventional elements for the power amplifiers.

Rubin discloses a conventional GaAs FET used for large signal operations (See column 2, line 32) thereby forming a power amplifier for RF applications (See column 1, lines 9 and 10).

Art Unit: 2817

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted a GaAs FET power amplifier for the power amplifier units of Mattila because, as the reference is silent as to the construction of the power amplifiers, any art-recognized equivalent power amplifier would have been usable such as the conventional GaAs FET power amplifier of Rubin wherein the input is applied as the gate thereof.

With respect to claims 13-20, Figures 1 and 2 of Mattila disclose a wireless communication device (See cellular telephone use recited in column 3) having an amplifier circuit (Figure 1) for amplifying a radio frequency (RF) signal, the RF signal comprising an amplitude modulated carrier having an amplitude modulation bandwidth, the amplifier circuit having a direct current (DC) bias voltage source (V_{ref} and V_{pwr}), a biasing circuit (Figure 2), the biasing circuit having an active element operational amplifier configured as a inverting amplifier N21 having an input connected to the DC bias voltage source and an output, wherein during its operation, i.e. during low and large signal inputs, due to the driver circuits like Q30 the active element inherently maintains a relatively low output impedance over a bandwidth comparable to the amplitude modulation bandwidth of the RIF signal and a resistor R31 having an input connected to the active element output and an output connected to the power amplifier, such that the DC bias voltage source provides a fixed DC voltage at the resistor input, regardless of voltage fluctuations of the RF signal received at the power amplifier. Alternatively, the selection of the bandwidth and the resistance value of the driver like Q30 so as to keep the operational amplifier N21 from saturating and thus keeping the output impedance thereof low is merely the selection of the optimum or workable range and as this involves routine skill in the art the selection of the bandwidth and resistance of the driver would have been obvious to one of ordinary skill in the art at the time the invention was made. Mattila is silent on the power amplifiers 3 having a transistor with an input for receiving the RF signal. Mattila does show generic conventional elements for the power amplifiers.

Rubin discloses a conventional GaAs FET used for large signal operations (See column 2, line 32) thereby forming a power amplifier for RF applications (See column 1, lines 9 and 10).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted a GaAs FET power amplifier for the power amplifier units of Mattila because, as the reference is silent as to the construction of the power amplifiers, any art-recognized equivalent power amplifier would have been usable such as the conventional GaAs FET power amplifier of Rubin. Note that the biasing circuit of Mattila combined with the GaAs FET of Rubin also forms "A gate bias circuit for biasing a gate of a field effect transistor..." as recited in claim 18.

Claims 21 and 26-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mattila et al. in view of Applicant's Admitted prior art as represented by Figure 1 (AAPA).

Art Unit: 2817

Figures 1 and 2 of Mattila disclose an amplifier circuit and associated method for amplifying a radio frequency (RF) signal (See abstract and column 3), the RF signal comprising an amplitude modulated carrier having an amplitude modulation bandwidth, having a direct current (DC) bias voltage source (V_{ref} and V_{pwr}), a biasing circuit (Figure 2), the biasing circuit having an active element operational amplifier configured as a inverting amplifier N21 having an input connected to the DC bias voltage source and an output, wherein during its operation, i.e. during low and large signal inputs, due to the driver circuits like Q30 the active element inherently maintains/"generates" a relatively low output impedance over a bandwidth comparable to the amplitude modulation bandwidth of the RF signal and a resistor R31 having an input connected to the active element output and an output connected/"coupled" to the power amplifier, such that the DC bias voltage source provides a fixed DC voltage at the resistor input, regardless of voltage fluctuations of the RF signal received at the power amplifier. Alternatively, the selection of the bandwidth and the resistance value of the driver like Q30 so as to keep the operational amplifier N21 from saturating and thus keeping the output impedance thereof low is merely the selection of the optimum or workable range and as this involves routine skill in the art the selection of the bandwidth and resistance of the driver would have been obvious to one of ordinary skill in the art at the time the invention was made. The bias amplifier of Mattila is a inverting buffering amplifier that inherently has a predetermined gain that is "relative" to the bias reference voltage. Since the bias amplifier is an non-inverting arrangement like that disclosed the bias amplifier arrangement of Mattila inherently sources and sinks current as needed to maintain a fixed bias voltage at the bias amplifier output even in the presence of signal disturbances feeding back from the bias input of the RF power device that are not blocked by the impedance between the RF device and the bias circuit. Mattila does not show the use of a reactive circuit composed of either an inductor device or 1/4 wavelength stub connected in series with a bias current limiting resistor such that this series combination is connected between the bias arrangement and the input of the RF device, and Mattila does not show the reactive circuit further includes a capacitance connected between the bias current limiting resistor and inductor or 1/4 wavelength stub and ground.

AAPA discloses the use of a reactive circuit composed of at least one inductor or 1/4 wavelength stub device 45 connected in series with a bias current limiting resistor 30 and having a capacitance 50 connected between the inductor device 45 and the resistor 30, and ground so as to block the RF signal from being feedback to or interfering with the bias circuit. Note that the bias limiting resistance 30 will inherently limit current to a maximum value (Note the second half of claims like claim 24).

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the arrangement of Mattila with a reactive circuit that is composed of at least an inductor device connected in series with a bias current limiting resistor, and having a capacitance connected between the inductor device and the bias current limiting resistance so as to block the RF signal from being feedback to or interfering with the bias circuit as taught by AAPA.

Claims 22-24 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over over Mattila et al. in view of Applicant's Admitted prior art as represented by Figure 1 (AAPA) as applied to claims 21 and 26-34 above, and further in view of Rubin et al. 4,320,352 (Rubin).

The reasoning as applied to claims 21 and 26-34 above and the following: Mattila is silent on the power amplifiers 3 having a transistor with an input for receiving the RF signal. Mattila does show generic conventional elements for the power amplifiers.

Rubin discloses a conventional common source GaAs FET used for large signal operations (See column 2, line 32 and note that the leg connected to ground of element 1 can be either the source or drain of the transistor.) thereby forming a power amplifier for RF applications (See column 1, lines 9 and 10). Rubin also includes the conventional DC blocking capacitor 3 connected between the signal input and the input of amplifier.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted a GaAs common source FET power amplifier for the power amplifier units of Mattila because, as the reference is silent as to the construction of the power amplifiers, any art-recognized equivalent power amplifier would have been usable such as the conventional GaAs FET power amplifier of Rubin wherein the input is applied as the gate thereof. Furthermore, it would have been obvious to one of ordinary skill in the art to add a blocking capacitor connected between the signal input and the RF amplifier in Mattila so as to block DC as taught by Rubin.

Response to Arguments

Applicant's arguments filed 5-19-2003 and 7-1-2003 have been fully considered but they are not persuasive.

In the arguments submitted in the after-final amendment dated 5-19-2003 it appears that applicant refers to the Mattila reference as "Jonas". Thus, it will be assumed that such is the case in response to these arguments. Applicant believes that Mattila does not disclose every element of the claimed invention and in particular applicant believes that "wherein during its operation the active element maintains a fixed

DC voltage at the resistor input” is not supported. This functional language does not set forth any positive limitation of structure and the examiner contends that the structure limitations are met by Mattila. Applicant explains that the output bias voltage will increase with increases in V_{pwr} and then makes a conclusion that “the output voltage of the active element is fixed and does not vary during its operation”. Applicant is not clear on what applicant means by “operation” for the examiner can not find any specific definition in the specification (See MPEP 2111.01), therefore, the examiner must give the broadest reasonable interpretation to the claims (MPEP 2111) and the words used in the claim must be given their plain meaning (MPEP 2111.01). In Mattila the value of V_{pwr} merely controls the desired system transmitting power level (See column 3, around line 65). Thus there is an “operation” where the transmitting power is kept constant through or during its “operation”. If V_{pwr} is kept constant then as explained previously the bias potential is kept constant. Applicant in the arguments presented in 7-1-2003 recites that the invention solves a problem of there being an undesired capacitance and that the active amplifier circuit of applicant’s invention acts as a “virtual capacitor” that is to “sink and source current as needed to quash unwanted signal disturbances...”. Applicant then concludes that “[n]one of the cited references disclose or even allude to the particular biasing problems being solved by the present invention and implementation of any or all of the circuits illustrated in the cited references would fail to solve that problem”. Applicant has not presented evidence why these features would not be inherent in Mattila as Mattila also employs an amplifier arrangement between the power source and the bias terminals of the active element that is being biased. The examiner also fails to see any arguments concerning the rejections based on optimization of parameters. Furthermore, at least some of the claims were rejected under 35 USC 102 and thus the structure is anticipated and items like unexpected results would possibly be persuasive in showing unobviousness but not under issues of anticipation.

Claim 25 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening

Art Unit: 2817

claims. The prior art fails to suggest or teach the use of a non-inverting amplifier for use in the bias arrangement combined with all the other claimed features.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael B. Shingleton whose telephone number is 703-308-4903. The examiner can normally be reached on Monday-Thursday from 8:30 to 4:30. The examiner can also be reached on alternate Fridays.

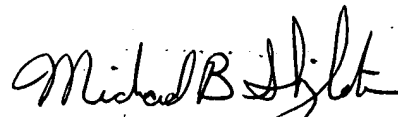
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal, can be reached on (703) 308-4909. The fax phone number for the organization where this application or proceeding is assigned is 703-308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

MBS

March 22, 2003

July 23, 2003


MICHAEL B SHINGLETON
PRIMARY EXAMINER
GROUP ART UNIT 2817